D 93435 (Pages : 3) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2020

(CBCSS)

Physics

PHY IC 04—ELECTRONICS

(2019 Admissions)

Time : Three Hours Maximum : 30 Weightage

General Instructions

1. *In cases where choices are provided, students can attend* **all** *questions in each section.*
2. *The minimum number of questions to be attended from the Section / Part shall remain the same.*
3. *There will be an overall ceiling for each Section / Part that is equivalent to the maximum weightage of the Section / Part.*

Section A

Answer **all** *questions, each carries weightage* 1.

1. Briefly explain any *two* ideal parameters of an operational amplifier.
2. How can you change the colours of emission in a LED ? Give any *two* examples for different colours.
3. Briefly explain fill factor and efficiency.
4. Distinguish between BJT and FET.
5. Briefly explain the advantages of Karnaugh map in logic circuit design..
6. Describe the working of a PN junction diode as a solar cell.
7. Write a short note on switching action of a MOSFET.
8. How can you convert an SR Flip-flop to a D Flip-flop ?

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions, each carries weightage* 5.

9. With the help of a logic circuit briefly explain the working of a decade counter.
10. How can you construct an active high pass filter using operational amplifier ? Explain its working.

Turn over

11. What is the use of positive feedback ? With the help of a circuit explain the working of a Wien bridge oscillator.

12. With the help of a circuit explain the conversion of an analog signal to digital signal.

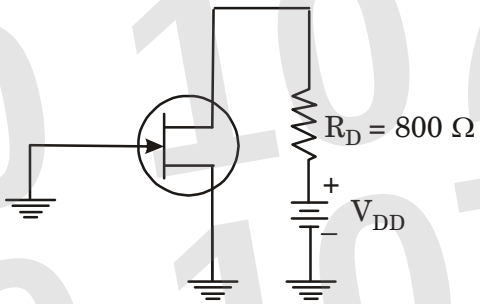
(2 × 5 = 10 weightage)

Section C

Answer any **four** *questions, each question carries weightage* 3.

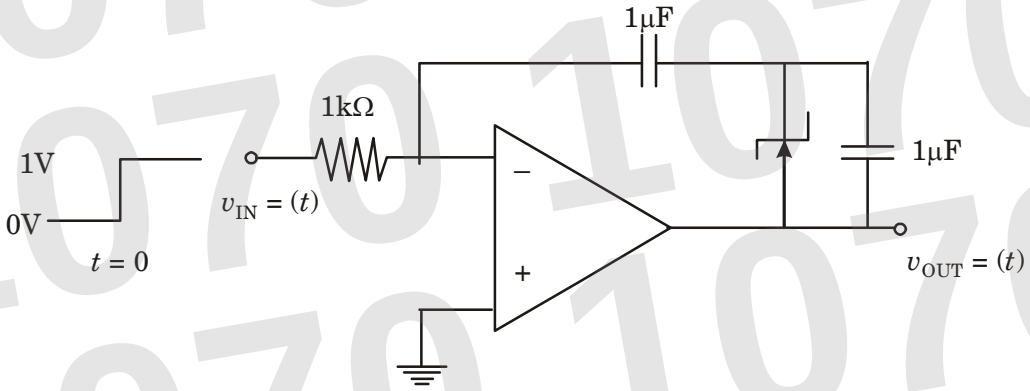
13. Design an Integrator that integrates signals with frequencies down to 200 Hz and produces a peak output of 0.5 V when the input used is a 25 V peak sine wave having frequency 20 kHz.

14. For the JFET in the given figure, $V_{GS\ (off)}$ is –4V and I_{DSS} is 10 mA. Determine the minimum value of V_{DD} required to put the device in constant current area of operation :



15. Design a first order Butterworth low pass filter circuit using operational amplifier with a cutoff frequency 15.9 kHz. C = 0.001 μ F and A_{max} = 1.5

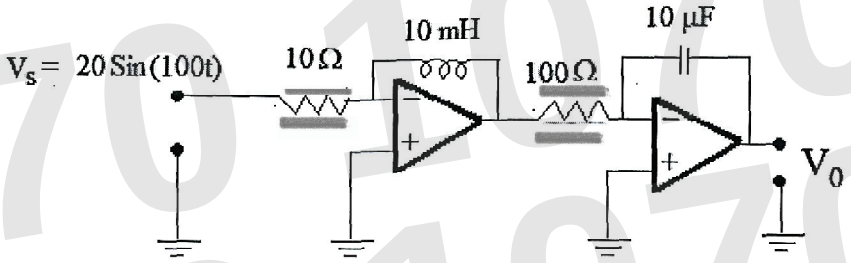
16. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied, *i.e. vin* (*t*) = *u* (*t*) volts. Also, at *t* = 0, the voltage across each of the capacitors is zero. Find the time '*t*' in milliseconds, at which the output voltage V_{out} crosses the Zener break down.



17. Using Karnaugh Map solve the given equation to reduce the number of gates used :

$$Y = \bar{A}\bar{B}CD + \bar{A}BCD + ABCD + A\bar{B}CD + AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D}.$$

18. In the figure given below assume the ideal op-amp is used. Find the output voltage if an input signal $V_s = 20 \text{ Sin } (100t)$ is applied.



19. Design an astable multi-vibrator using operational amplifier to get 500 Hz.

(4 × 3 = 12 weightage)